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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2133	3

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/027,311	Applicant(s) ANDREEV ET AL.	
	Examiner John P Trimmings	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-18 and 21* is/are rejected.

7)☒ Claim(s) *4,5,19 and 20* is/are objected to.

8)☒ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-21 are presented for examination.

Information Disclosure Statement

The examiner acknowledges the applicant's Information Disclosure of 2/26/2002.

Drawings

1. The drawings are objected to because FIG.1 Test Circuit 100 is not labeled "100". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to because FIG.5C box 552 does not have an exit line to "C". Also, box 548 has 2 exit lines. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. New corrected drawings are required in this application because the drawings are hand-drawn and are not in publishable form. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities:

Page 7 line 14 recites, "multiplexers 202, 204, 206, 208, and 210", but the examiner believes it should read, "multiplexers 206, 208, 210, 212, and 214".

Page 7 line 17 recites, "multiplexer 202", but the examiner believes it should read, "multiplexer 206".

Page 7 line 21 recites, "multiplexer 204", but the examiner believes it should read, "multiplexer 208".

Page 7 line 23 recites, "multiplexer 206", but the examiner believes it should read, "multiplexer 210".

Page 7 line 25 recites, "multiplexer 208", but the examiner believes it should read, "multiplexer 212".

Page 7 line 28 recites, "multiplexer 210", but the examiner believes it should read, "multiplexer 214".

Page 8 line 20 recites, "signals 218", but the examiner believes it should read, "signals 219".

Appropriate correction is required.

Claim Objections

5. Claims 1 and 15 are objected to because of the following informalities: the claims recite "as few as 7 control lines", which is not a positive limitation to the claim. The

examiner believes that "7 or more control lines" would convey a positive limitation. Appropriate correction is required.

6. Claim 21 is objected to because of the following informalities: there is one too many "if"s in line 3 of the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 3 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim specifies that a "START" signal and "MBIST_GO" is a control signal between the controller and collar, but this conflicts with the specification and drawings. The two signals are not part of the 7 control signals between controller and collar, or a switching signal, or a test vector.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 15 and 2, 16 are rejected under 35 U.S.C. 102(b) as being anticipated by M. Lobetti Bodoni et al., "An Effective Distributed BIST Architecture for RAMs".

As per Claim 1 and 15:

Lobetti et al. teaches a memory test circuit or method (see Abstract) comprising: a collar for coupling to a memory device (page 119 column 2 1st paragraph) for switching an address bus and a data bus of the memory device (see FIG.2 Address/Data multiplexers) between an external circuit and the collar in response to a switching signal (mode status bit and page 121 column 1 last paragraph and column 2); and a controller coupled to the collar for generating the switching signal (mode status bit is loaded from BIST Processor as in FIG.2 or 3), a test vector, and control signals on as few as seven control lines between the controller and the collar for testing the memory device with the test vector (page 122 column 1, and FIG.2 shows 7 signals).

As per Claim 2 and 16:

Lobetti et al. teaches the memory test circuit of Claim 1 wherein the controller (FIG.3 BIST Processor) generates the control signals for multiple memory devices of various sizes (page 119 column 2 paragraph 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 3, 6-9, 11-14, 17, 18 and 21are rejected under 35 U.S.C. 103(a) as being unpatentable over M. Lobetti Bodoni et al., "An Effective Distributed BIST Architecture for RAMs", and further in view of Kraus et al., U.S. Patent No. 6587979.

As per Claim 3 and 17:

Lobetti et al. fails to further teach the memory test circuit of Claim 1 wherein the control signals are further specified. However, in an analogous art, Kraus et al. does supply the collar with control signals from a BIST controller (FIG.16 100), comprising a

"CLEAR" signal (FIG.16 RESET), a "NEXT" signal (FIG.16 COL or ROW CLOCK), a "TEST ENABLE" signal (FIG.16 MODE), a "START" signal (FIG.6 START note: this is an external signal and has been rejected under 35 USC 112 1st), a "WRITE ENABLE" signal (FIG.16 CNT), a "MOVE" signal (FIG.16 DATA CLOCK), a "D" signal (FIG.16 ENCODED DATA), a "MBIST GO" signal (FIG.6 START note: this is an external signal and has been rejected under 35 USC 112 1st), and a "TEST IN" signal (FIG.16 CERR). One with ordinary skill in the art would find it obvious to apply the control signals used with Kraus et al. into the system specified by Lobetti et al. after finding that Lobetti et al. did not specifically name the control signals. And Kraus et al., in column 2 lines 32-40 recites an advantage to be an easy implementation of BIST circuits to handle varying numbers and sizes of memories. One with ordinary skill in the art at the time of the invention, motivated as suggested by Kraus et al., would combine the references.

As per Claim 6:

Lobetti et al. further teaches the memory test circuit of Claim 3 wherein the collar comprises a multiplexer coupled to the address bus of the memory device and the "TEST ENABLE" signal (see FIG.2 and Mode Status bit in page 121 column 2 3rd paragraph). And in view of the motivation previously recited, the claim is rejected.

As per Claim 7:

Lobetti et al. further teaches the memory test circuit of Claim 6 wherein the collar comprises an address register coupled to the multiplexer (FIG.2 Address Generator). And in view of the motivation previously recited, the claim is rejected.

As per Claim 8:

Kraus et al. further teaches the memory test circuit of Claim 7 wherein the address register is reset to zero by the "CLEAR" signal (column 13 lines 1-11 and column 17 lines 17-21). And in view of the motivation previously recited, the claim is rejected.

As per Claim 9:

Kraus et al. further teaches the memory test circuit of Claim 8 wherein the address register is incremented by the "NEXT" signal (column 17 lines 21-30). And in view of the motivation previously recited, the claim is rejected.

As per Claim 11:

Lobetti et al. further teaches the memory test circuit of Claim 6 wherein the collar comprises a data register coupled to the multiplexer for writing a test vector into the memory device (FIG.2 Background Pattern Generator). And in view of the motivation previously recited, the claim is rejected.

As per Claim 12:

Kraus et al. further teaches the memory test circuit of Claim 11 wherein the test vector is transferred to the data register by the "MOVE" signal (FIG.16 DATA CLOCK) and the "D" signal (FIG.16 ENCODED DATA). And in view of the motivation previously recited, the claim is rejected.

As per Claim 13:

Kraus et al. further teaches the memory test circuit of Claim 11 wherein the collar comprises a data comparator (FIG.6 52) coupled to the data register (FIG.6 50) and to

the memory device (FIG.6 DO) for generating the "TEST IN" signal (FIG.6 CERR). And in view of the motivation previously recited, the claim is rejected.

As per Claims 14 and 21:

Lobetti et al. further teaches the memory test circuit of Claim 3 wherein the "MBIST GO" signal (page 121 column 2 last paragraph – "GO") has an initial value of one and is latched to zero upon detection of a memory device error. And in view of the motivation previously recited, the claim is rejected.

As per Claim 18:

Lobetti et al. further teaches the method of Claim 17 wherein the switching signal is the "TEST ENABLE" signal (mode status bit, see page 121 column 2). And in view of the motivation previously recited, the claim is rejected.

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over M. Lobetti Bodoni et al., "An Effective Distributed BIST Architecture for RAMs", and in view of Kraus et al., U.S. Patent No. 6587979 as applied to Claim 7, and further in view of Kornachuk et al., U.S. Patent No. 6044481. Kraus et al. further teaches the memory test circuit of Claim 7 wherein the collar comprises an address comparator coupled to the address register (FIG.13 COMP 84) but fails to teach that the comparator generates a memory enable signal. However, in an analogous art, Kornachuk et al. does control memory enable (signals TCE, TIS, CE, CEQ in FIG.2C) under address control (see Appendix D). It would have been obvious to one with ordinary skill in the art to modify the control signals (that were not specified in Lobetti et al.) to disable the memory under

test if "EOAD" (end of address, page 121 column 2) went high. And Kornachuk et al., recites in column 2 lines 24-67 and column 3 lines 1-2 the advantage of a highly adaptive programmable interface without the need to customize a collar in a memory test system. And one with ordinary skill in the art at the time of the invention, motivated by Kornachuk et al., would combine the references.

Allowable Subject Matter

11. Claims 4, 5, 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

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